ZEKE Platform

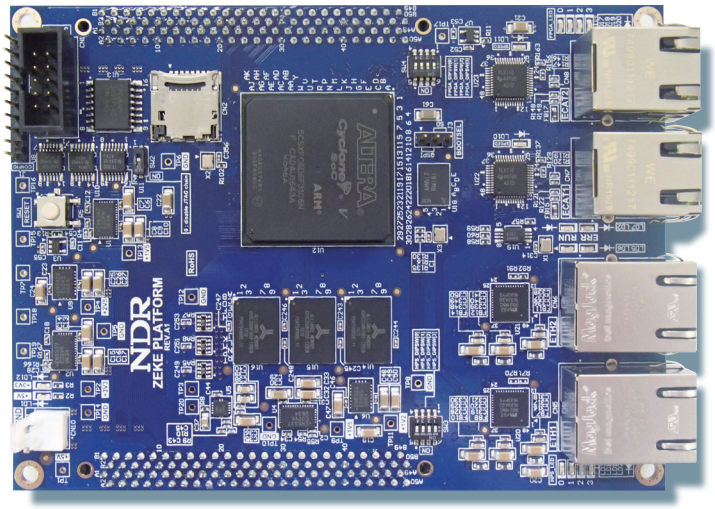
FPGA Design Solutions Network

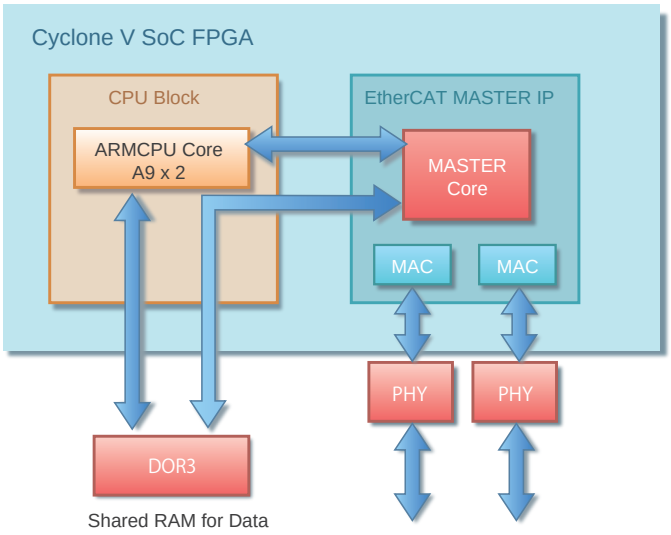
High performance platform for industrial equipment with Intel Cyclone V SoC

The ZEKE Platform is developed mainly for Industrial Ethernet applications.

Cyclone V SoC

- High performance CPU board with Arm Cortex A9 x 2 @ 925 MHz on which Linux etc. can be used in SMP mode.
- The only board in which both Gbit EtherNET ports of the Arm can be used.
- Since two 10/100 PHYs are implemented in the FPGA, TSE MAC from Intel Corporation can be used.





● EtherCAT Hardware Master Block Diagram

EtherCAT® Implementation

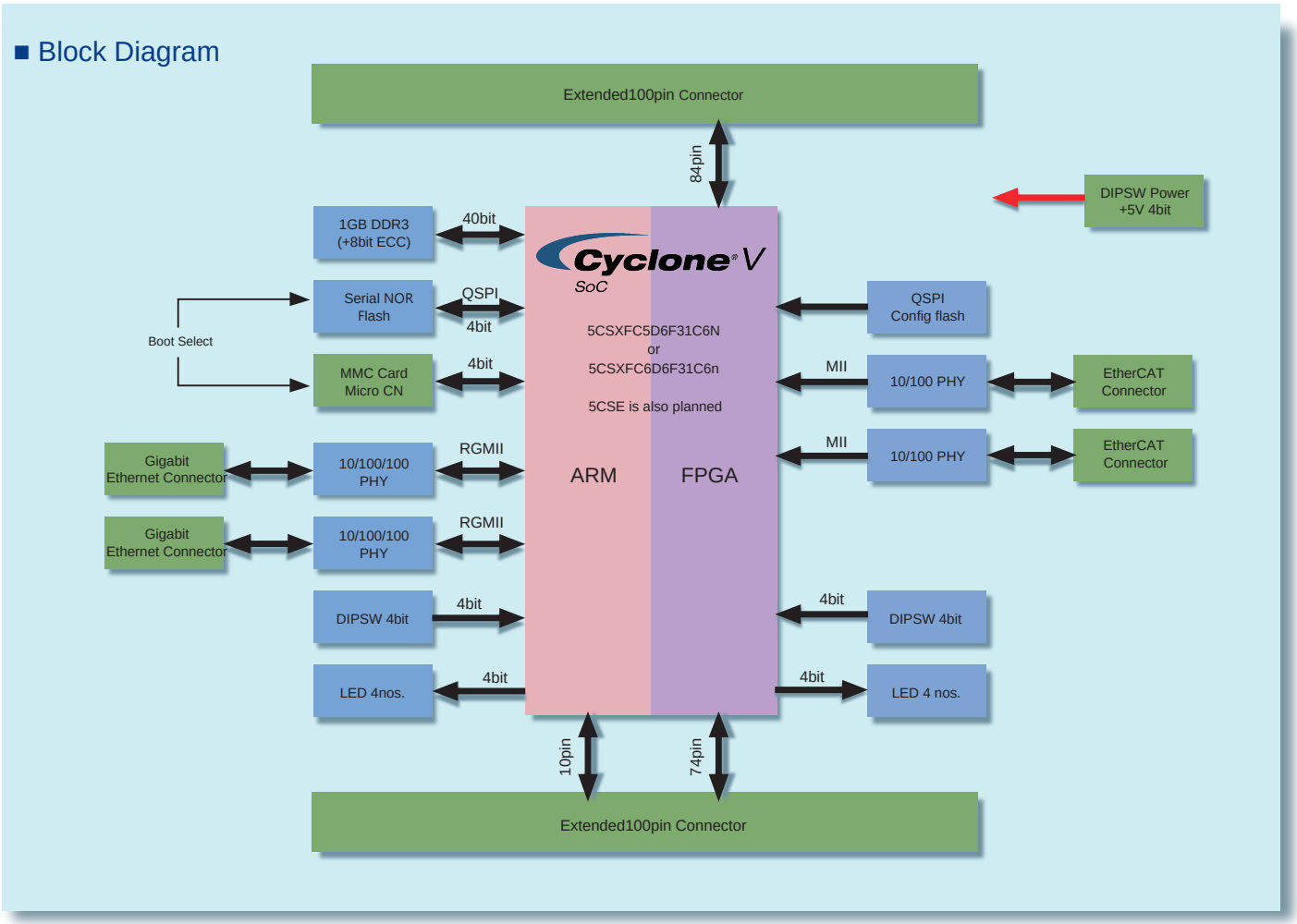
- **Hardware Master**
  It is possible to evaluate our hardware master using ethernet of the FPGA.

- **Software Master**
  It is possible to implement paid software masters from various companies using the ethernet of the Arm.
  We also provide the demo environment for implementing the Open source Master stack.

- **Slave**
  Ethernet of the FPGA can also be used as a slave by implementing BECKHOFF EtherCAT slave IP etc.

NDR

■ Block Diagram



■ Specifications

Core specifications		
FPGA+SoC	Cyclone V series (Dual core Arm Cortex-A 9 925 MHz)	5CSXFC6D6F31C6N/5CSXFC5D6F31C6N
		5CSEMA6F31C6N/5CSEMA5F31C6N
	Config flash	EPCQ64SI16N
Power supply	Input : 5.0V	Supplied from power connector (B2P-VH) or extension connector
	Output : 3.3V	3.3 V output from an extension connector (assumed to be used as a power supply for a tolerant buffer)
Clock	25MHz	3 Units mounted (1 each of ARM, FPGA, PHY)
GPIO	2 No.s of 1.27 25x4 rows of staggered connectors	FX2C-100S-1.27DSA (Hirose Electric make)
	Each connector with 84 CH (Total 168 CH)	CN 4 : FPGA unit 84 CH, CN 9 : FPGA unit 74 CH, HPS unit 10 CH
Ethernet	Gigabit Ethernet (2CH):HPS	CN5, CN6PHY : KSZ9021RNI
	100base Ethernet (2CH) : FPGA	CN7, CN8 PHY : TLK110PTR
LED	POWER LED	2 units (5.0 V, 3.3 V)
	USER LED (Total 168 CH)	8 units(HPS : 4 green units, FPGA : 4 green units)
	EtherCAT LED (Total 168 CH)	HPS : RUN (1 green unit), ERR (1 red unit), FPGA : RUN (1 green unit), ERR (1 red unit)
DIP Switch	2 out of 4 units loaded	HPS : 1 unit (SW 3), FPGA : 1 unit (SW 4)
Push switch	1 unit	Reset switch (SW1)
JTAG	Connector	1 unit (CN1)
		Can be set to FPGA only or FPGA+HPS using the Slide switch (SW2)
Memory	DDR3	256Mx32bit, 8bit ECC 400MHz : AS4C256M16D3A-12BCN
	QSPI flash	521Mbit(64Mx8bit) : MT25QL512ABB8E12-0SIT *1
	Micro SD	Used as a drive by inserting the card into the MicroSD Slot (CN2) *2
*1 *2 Can be used as boot memory; boot memory can be selected by J3.		

NDR | NDR Co., Ltd.

Contact Us URL . http://www.ndr.co.jp/ E-mail. info-ndr@ndr.co.jp

2F, Sumitomoseimei Minatomachi MT Bldg ., 1-18-4 , Minamihorie, Nishi-Ku, Osaka, Japan 550-0015

Business overview: NDR manufactures mass production boards from prototype development for industrial equipment. Development of FPGA on digital signal processing board, Analog/Digital board and the CPU board that are mounted especially on Linux and RTOS, and development of ASSP of dedicated specification and replacement functionality of IC with soft-compatible FPGA for the discontinued IC' s is carried out.